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TECHNICAL DATA

MC145407

Advance Information

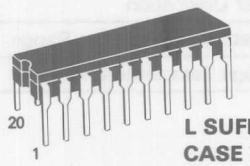
5-Volt-Only Driver/Receiver
EIA-232-D and CCITT V.28

The MC145407 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA-232-D and CCITT V.28 while operating from a single +5 volt power supply. A voltage doubler and inverter convert the +5 volts to ±10 volts. This is accomplished through an on-board 20 kHz oscillator and four inexpensive external electrolytic capacitors. The three drivers and three receivers of the MC145407 are virtually identical to those of the MC145406. Therefore, for applications requiring more than three drivers and/or three receivers, an MC145406 can be powered from an MC145407, since the MC145407 charge pumps have been designed to guarantee ±5 volts at the output of up to six drivers. Thus the MC145407 provides a high-performance, low-power, stand-alone solution or, with the MC145406, a +5 volt-only, high-performance two-chip solution.

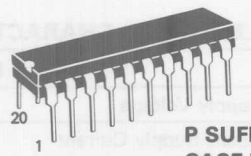
Drivers
- ±7.5 Volt Output Swing
- 300 Ohms Power-Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Slew Rate Range Limited from 4 V/μs to 30 V/μs

Receivers
- ±25 Volt Input Range
- 3 to 7 Kilohms Input Impedance
- 0.8 Volt Hysteresis for Enhanced Noise Immunity

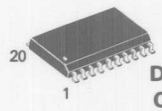
Charge Pumps
- +5 Volts to ±10 Volt Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three On-Chip Drivers and Three Drivers on the MC145406 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On-Chip 20 kHz Oscillator



L SUFFIX
CASE 732
CERAMIC

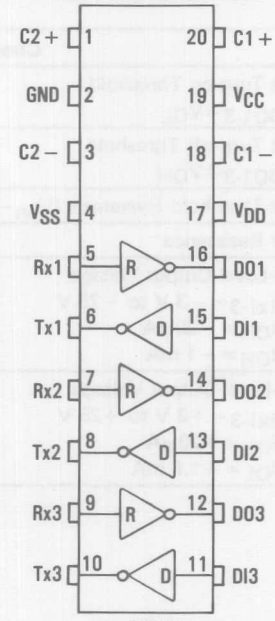


P SUFFIX
CASE 738
PLASTIC



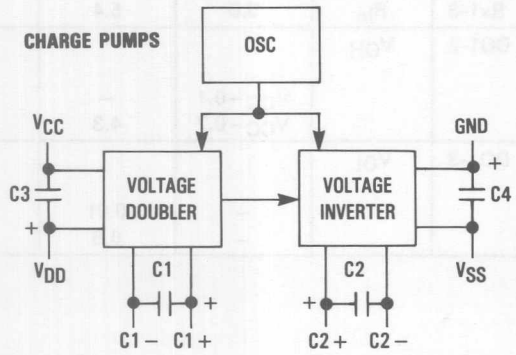
DW SUFFIX
CASE 751D
SOIC

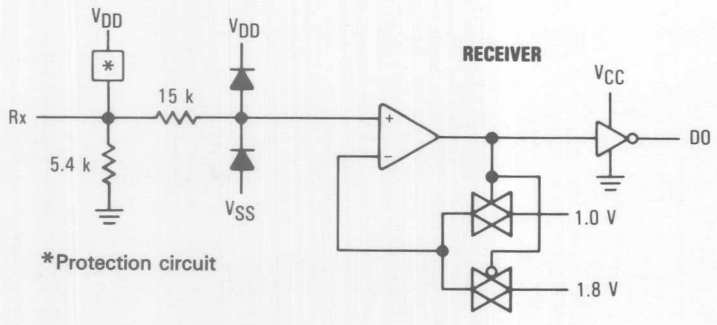
PIN ASSIGNMENT

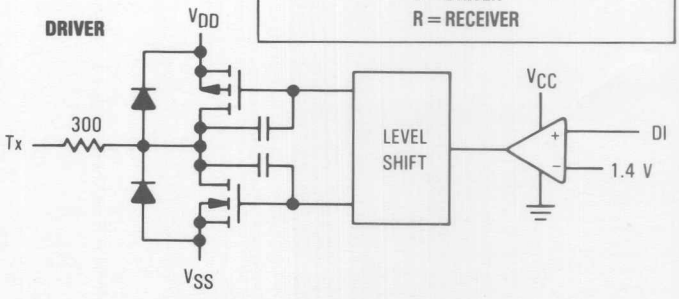


D = DRIVER
R = RECEIVER

FUNCTION DIAGRAM







This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{CC}	−0.5 to 6.0	V
Input Voltage Range Rx1-3 Inputs DI1-3 Inputs	V_{IR}	 $V_{SS}-15$ to $V_{DD}+15$ −0.5 to ($V_{CC}+0.5$)	V
DC Current Per Pin	I	±100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \le V_{DI} \le V_{DD}$ and $GND \le V_{DO} \le V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS}-15\ V) \le V_{Rx1-3} \le (V_{DD}+15\ V)$, and Tx should be constrained to $V_{SS} \le V_{Tx1-3} \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V; CI, C2, C3, C4 = 10 μF; T_A = −40 to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Outputs unloaded, inputs low)		I_{CC}	—	1.2	3.0	mA
Output Voltage	I_{load} = 0 mA	V_{DD}	8.5	10	11	V
	I_{load} = 5 mA		7.5	9.5	—	
	I_{load} = 10 mA		6	9	—	
	I_{load} = 0 mA	V_{SS}	−8.5	−10	−11	
	I_{load} = 5 mA		−7.5	−9.2	—	
	I_{load} = 10 mA		−6	−8.6	—	

RECEIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V; V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn-on Threshold $V_{DO1-3} = V_{OL}$	Rx1-3	V_{on}	1.35	1.8	2.35	V
Input Turn-off Threshold $V_{DO1-3} = V_{OH}$	Rx1-3	V_{off}	0.75	1.0	1.25	V
Input Threshold Hysteresis ($V_{on} - V_{off}$)	Rx1-3	V_{hys}	0.6	0.8	—	V
Input Resistance	Rx1-3	R_{in}	3.0	5.4	7.0	kΩ
High-Level Output Voltage V_{Rx1-3} = −3 V to −25 V I_{OH} = −20 μA I_{OH} = −1 mA	DO1-3	V_{OH}	 $V_{CC}-0.1$ $V_{CC}-0.7$	 — 4.3	 — —	V
Low-Level Output Voltage V_{Rx1-3} = +3 V to +25 V I_{OL} = +20 μA I_{OL} = +1.6 mA	DO1-3	V_{OL}	 — —	 0.01 0.5	 0.1 0.7	V

DRIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V; V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1-3					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2.0	—	—	
Input Current $GND \leq V_{DI1-3} \leq V_{CC}$	DI1-3	I_{in}	—	—	±1.0	μA
Output High Voltage	Tx1-3	V_{OH}	6	7.5	—	V
V_{DI1-3} = Logic 0, R_L = 3.0 kΩ	Tx1-6*		5	6.5	—	
Output Low Voltage	Tx1-3	V_{OL}	−6	−7.5	—	V
V_{DI1-3} = Logic 1, R_L = 3.0 kΩ	Tx1-6*		−5	−6.5	—	
Off Source Impedance (Figure 1)	Tx1-3	Z_{off}	300	—	—	Ω
Output Short-Circuit Current	Tx1-3	I_{SC}				mA
V_{CC} = +5.5 V						
Tx1-3 shorted to GND**			—	—	±60	
Tx1-3 shorted to ±15 V***			—	—	±100	

*Specifications for an MC145407 powering an MC145406 with three additional drivers/receivers.

**Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

***This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = −40 to 85°C; See Figures 2 and 3)

Characteristic		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1-3	t_{PLH}				μs
Low-to-High						
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			—	0.5	1	
High-to-Low		t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			—	0.5	1	
Output Slew Rate	Tx1-3	SR				V/μs
Minimum Load						
R_L = 7 kΩ, C_L = 0 pF			—	±6	±30	
Maximum Load						
R_L = 3 kΩ, C_L = 2500 pF			—	±5.0	—	
Receivers (C_L = 50 pF)						
Propagation Delay Time	DO1-3					μs
Low-to-High		t_{PLH}	—	—	1	
High-to-Low		t_{PHL}	—	—	1	
Output Rise Time	DO1-3	t_r	—	250	400	ns
Output Fall Time	DO1-3	t_f	—	40	100	ns

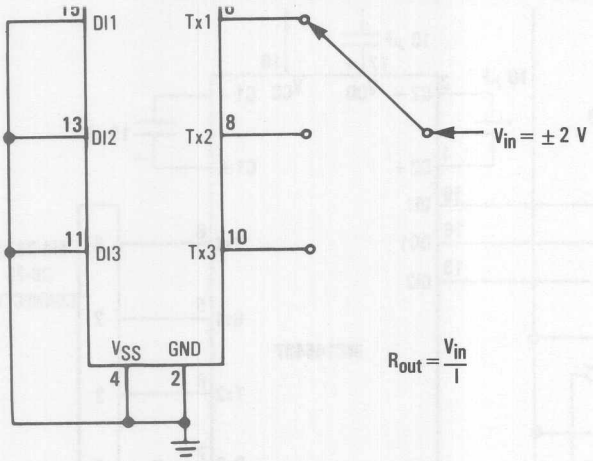


Figure 1. Power-Off Source Resistance

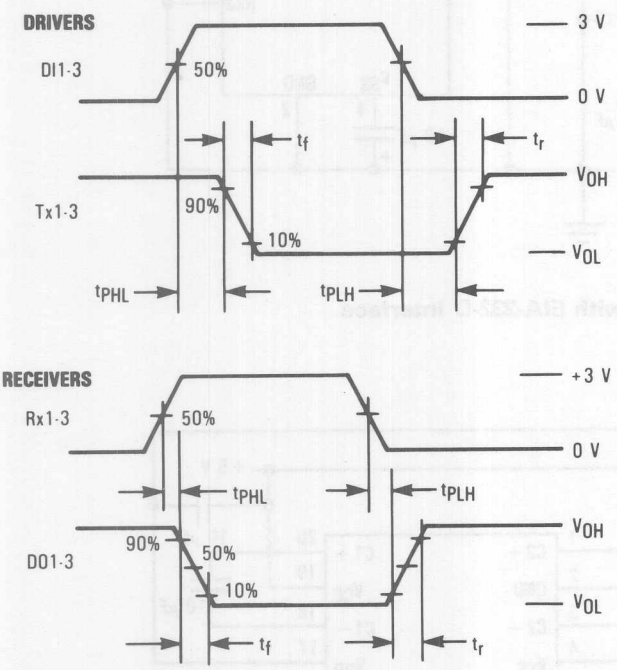


Figure 2. Switching Characteristics

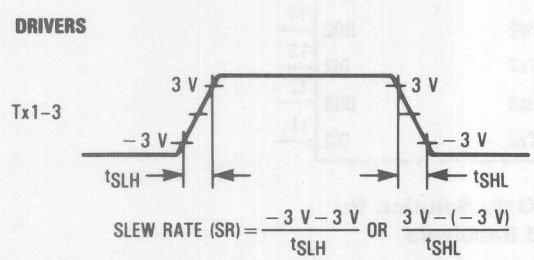


Figure 3. Slew Rate Characteristics

The digital supply pin, which is connected to the logic power supply. This pin should have a 0.33 μF capacitor to ground.

GND—GROUND (PIN 2)

Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (connector pin 7) as well as to the logic power supply ground.

V_{DD}—POSITIVE POWER SUPPLY (PIN 17)

This is the positive output of the on-chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}—NEGATIVE POWER SUPPLY (PIN 4)

This is the negative output of the on-chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

C2+, C2−, C1−, C1+—VOLTAGE DOUBLER AND INVERTER (PINS 1, 3, 18, 20)

These are the connections to the internal voltage doubler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2, Rx3—RECEIVE DATA INPUT (PINS 5, 7, 9)

These are the EIA-232-D receive signal inputs. A voltage between +3 and +25 volts is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between −3 and −25 volts is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2, DO3—DATA OUTPUT (PINS 16, 14, 12)

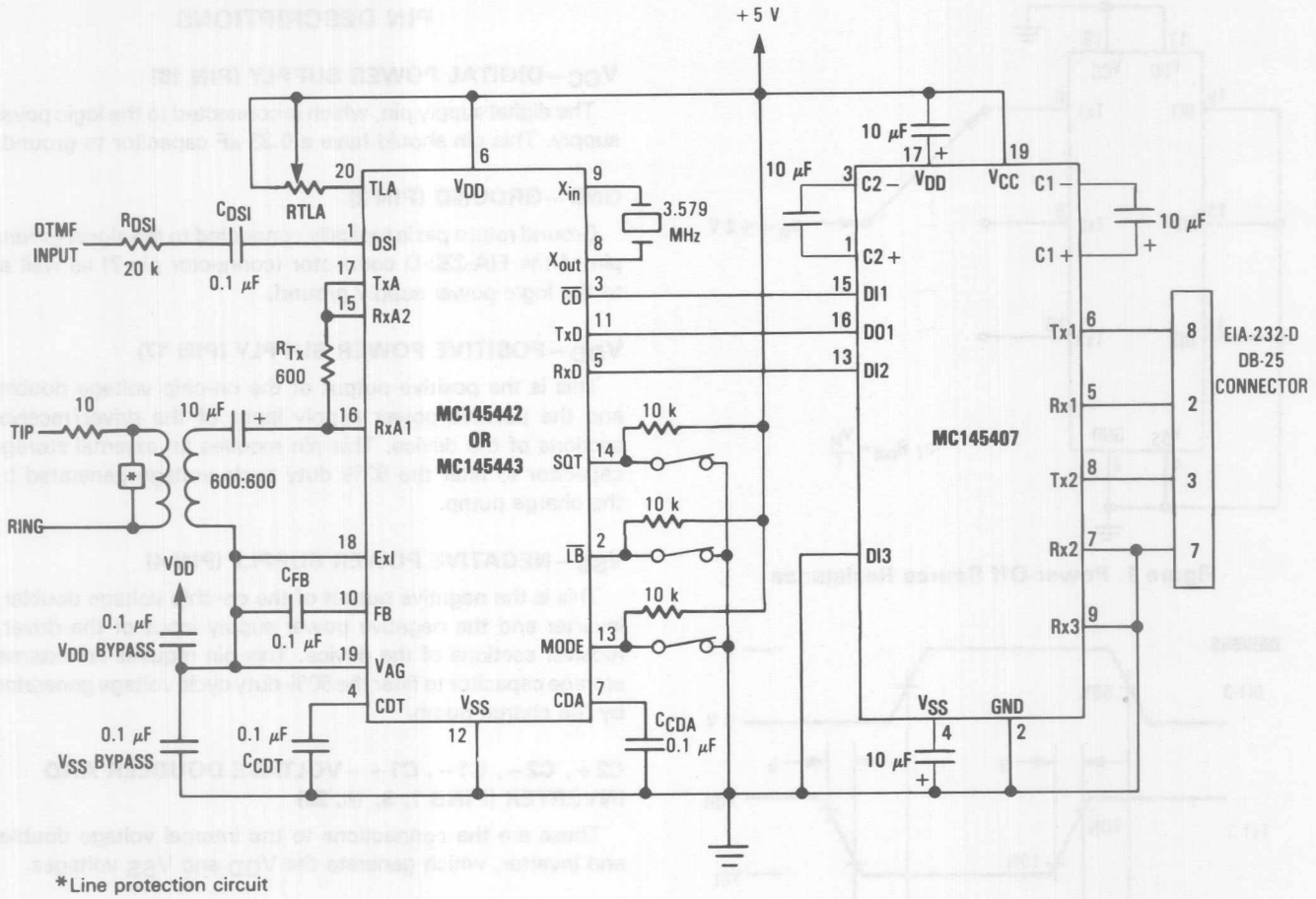
These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3—DATA INPUT (PINS 15, 13, 11)

These are the high-impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3—TRANSMIT DATA OUTPUT (PINS 6, 8, 10)

These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corrresponding Tx output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD}. The actual levels and slew rate achieved will depend on the output loading ($R_L \| C_L$).



*Line protection circuit

Figure 4. 5-Volt 300-Baud Modem with EIA-232-D Interface

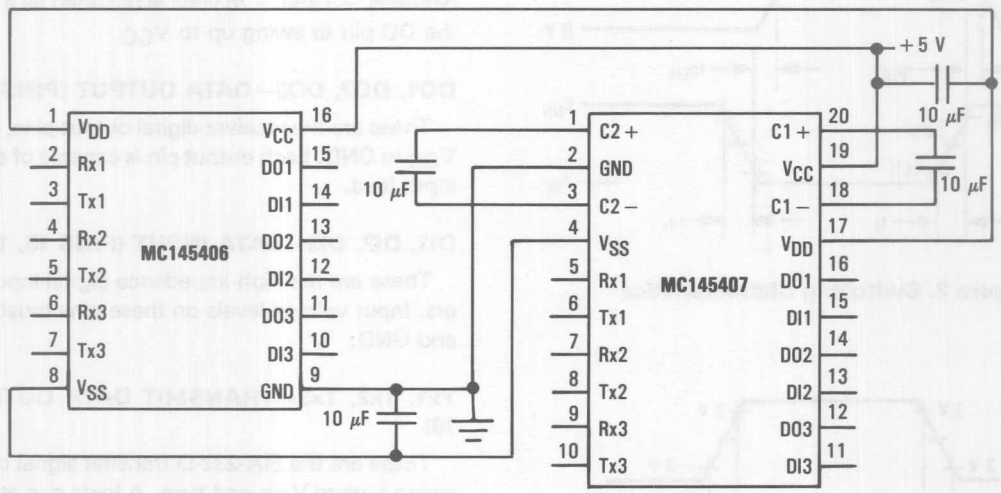
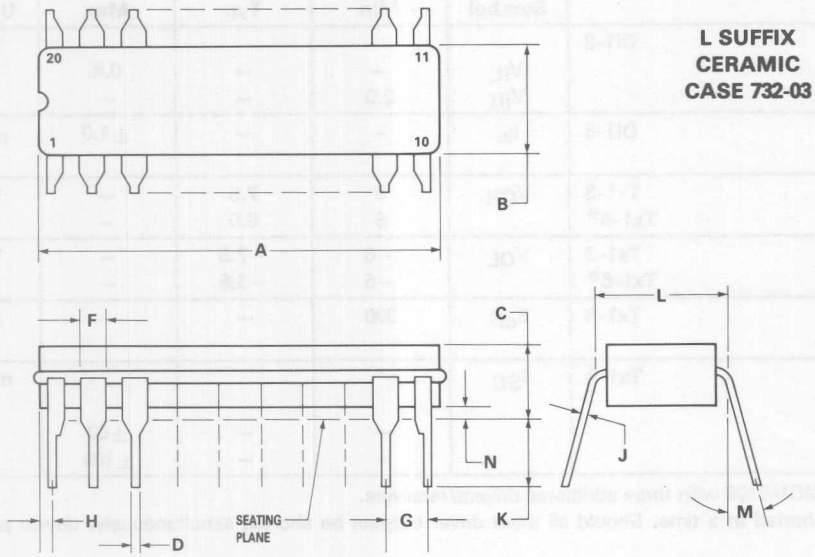


Figure 5. MC145406/MC145407 5-Volt-Only Solution for up to Six EIA-232-D Drivers and Receivers

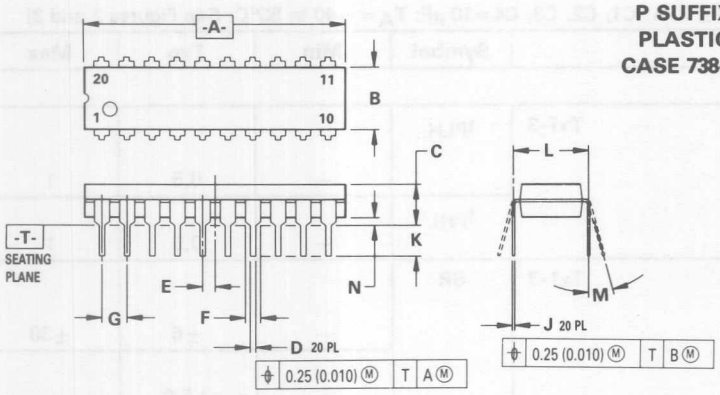
PACKAGE DIMENSIONS



L SUFFIX
CERAMIC
CASE 732-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

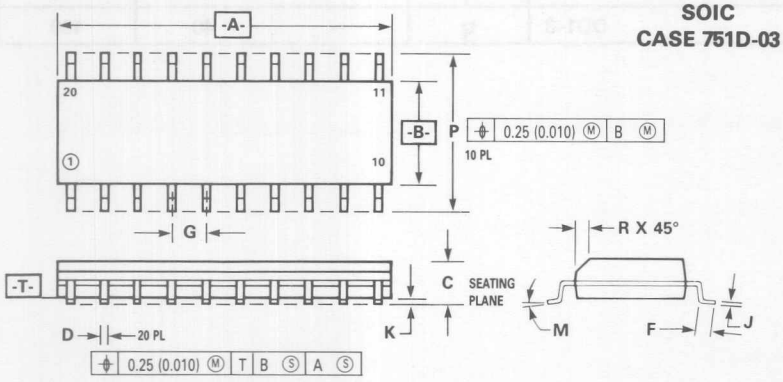
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.



P SUFFIX
PLASTIC
CASE 738-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.



DW SUFFIX
SOIC
CASE 751D-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.65	12.95	0.499	0.509
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

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